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Technology of Real-World Analyzers (TAUR) and its practical application

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Abstract: The article describes the most important details of the project for reconfigurable construction of dedicated electronic machines intended for performing analyses of phenomena that occur in multi-component systems containing at least several million mutually interacting elements. Devices built in the presented technology can be characterized by the use of reconfigurable integrated circuits, spatial construction ensuring scalability, a redundant panel system as well as specially developed data transmission and work control systems. Machines work in a parallel manner and can solve problems in various fields of science and technology by competing with the speed of data processing with the latest supercomputing systems. As an example, we present details of the ARUZ machine containing 26,000 FPGAs, which was made using this technology.

Key words: Field Programmable Gate Array, parallel data processing, Technology of Real-World Analyzers, molecular simulations, topology of the network connections

I. INTRODUCTION

In the years 1999–2000, the concept of building a dedicated electronic analyzer of phenomena occurring in complex liquids was developed at Lodz University of Technology. Technology of Real-World Analyzers (in Polish: Technologia Analizatorów Układów Rzeczywistych – TAUR) was developed in the framework of research projects leading to construction of two prototype machines – KDLL [1, 2] and mDLL [3–5]. They were used to test key mechanisms responsible for the operation of the system. As a result of many years of research and testing, a technology to build Real-World Analyzers was developed. Devices built in this technology can contain up to several hundred million operational cells placed in three-dimensional network nodes. These machines can support solving problems from various fields of science and technology as well as other fields such as artificial intelligence, data encryption or issues re-

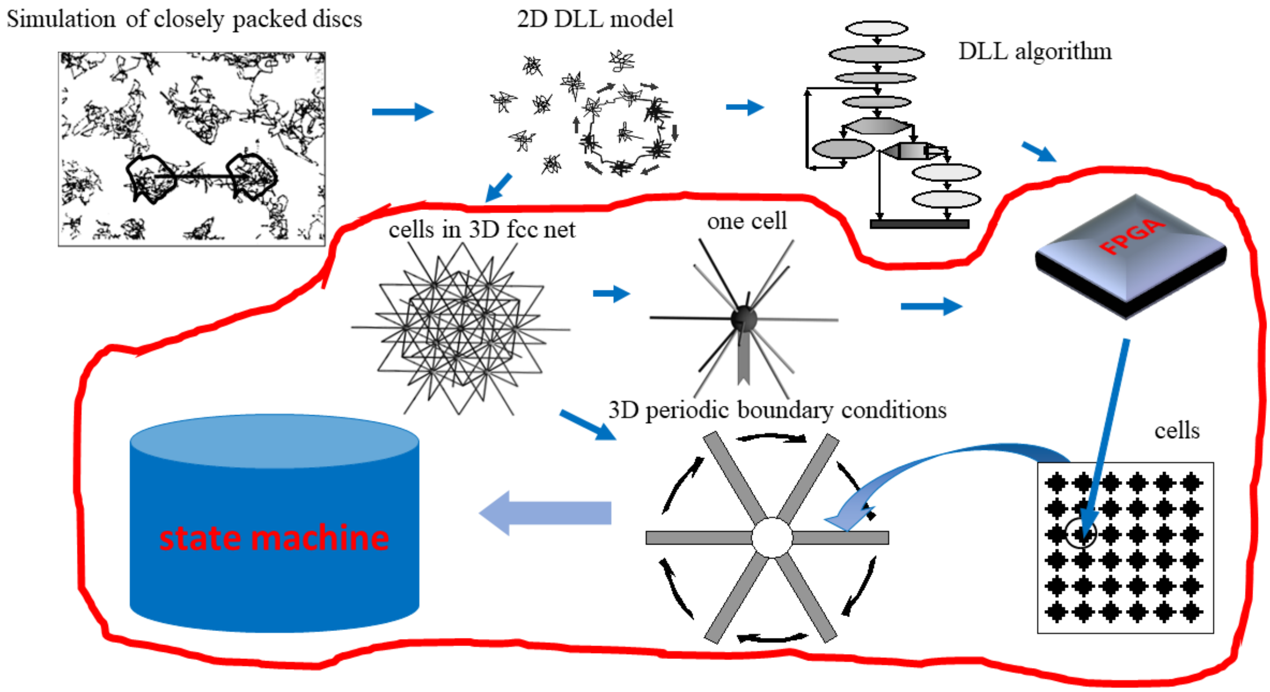

Fig. 1. Implementation of the DLL algorithm leading to TAUR technology

lated to military applications. Their common feature can be described as solving problems involving systems which consist of a large number of objects locally interacting with each other. All these objects perform activities simultaneously depending on their internal state, the condition of their nearest environment and states on external signal lines. TAUR emerged from studies of the Dynamic Lattice Liquid (DLL) algorithm which was applied for studies of the structure and dynamics of many soft matter systems [6–7].

II. PROPERTIES OF TAUR

The most important objects in machines built with the use of TAUR technology are operational cells. They perform a series of logical operations in one system clock cycle. The complexity of such operations is much greater than single arithmetic-logic operation in classic microprocessors. This implies that the operational cells process many times more information than microprocessors in a unit of time. In contrast to supercomputers consisting of a large number of concurrently operating microprocessors, machines made in TAUR can be seen as a huge macro-processor with features of a cellular automaton.

The most important characteristics of TAUR are as follows:

1. The devices consist of vertically arranged flat panels containing printed circuit boards (PCB) that consist of 8 Field Programmable Gate Arrays (FPGA) or Application-Specific Integrated Circuit (ASIC) integrated circuits [4(a), 4(b), 4(e)] (see Fig. 2).
2. In the integrated circuits operational cells are implemented in nodes of virtual face-centered cubic network (FCC) with coordination number 12 [4(c), 4(f), 4(h)] (Fig. 3).
3. FPGA (or ASIC) circuits on PCBs communicate with neighboring FPGAs on PCBs independently of the central control system via bidirectional signal lines [4(d), 4(g)] (red and blue lines in Fig. 2 and Fig. 4).
4. The network of operational cells can create a pseudo-infinite system (with periodic boundary conditions), while further expansion of the system will not cause delays in signal transmission between any neighboring operational cells [4(a), 4(b)] (Fig. 5).
5. All operational cells operate simultaneously (a parallel machine) and their work is synchronized via the central control system [4(c), 4(f), 4(h)] (marked in Fig. 6).
6. The results of the data processing process read out from internal registers of operational cells are sent via servers to the memory divided into modules assigned to individual panels. The readings take place at intervals selected by the system user (see Fig. 6).

7. PCBs are mounted on vertically placed water-cooled heat radiators. Vertical placement of radiators facilitates heat convection [4(a), 4(b)] (Fig. 2 – gray rectangles).

8. In the case of a breakdown, it is possible to continuously operate the system while repairing damaged elements (a redundant system of panels evenly arranged in a radial way) [4(e)] (Fig. 7).

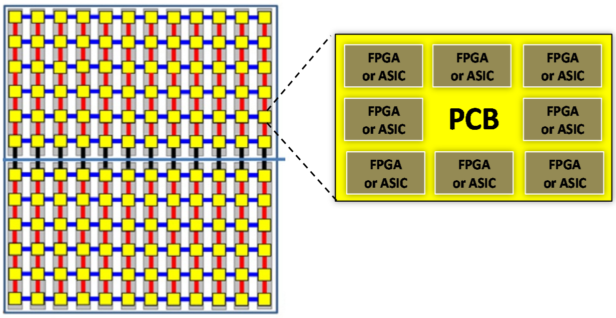

Fig. 2. A single panel with PCB (yellow squares) and a single PCB consisting of 8 FPGAs integrated circuits (or ASICs)

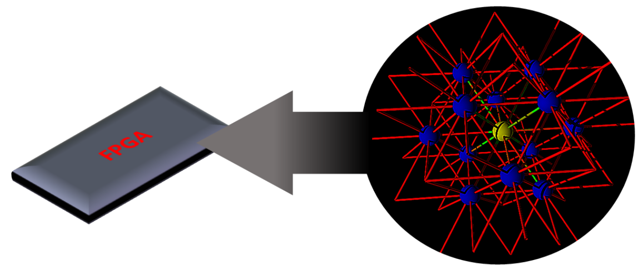

Fig. 3. A part of a FCC network containing 13 nodes implemented in an integrated circuit

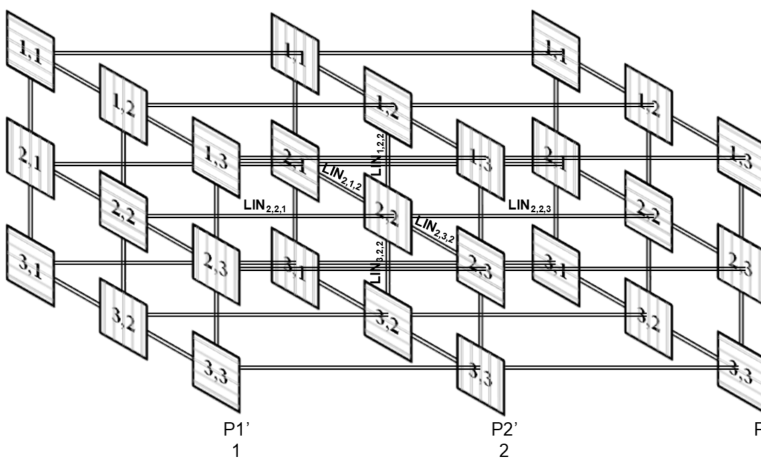

Fig. 4. Bidirectional communication lines between PCBs. Numbers indicate FPGAs (or ASICs) coordinates, while layers represent neighboring PCBs

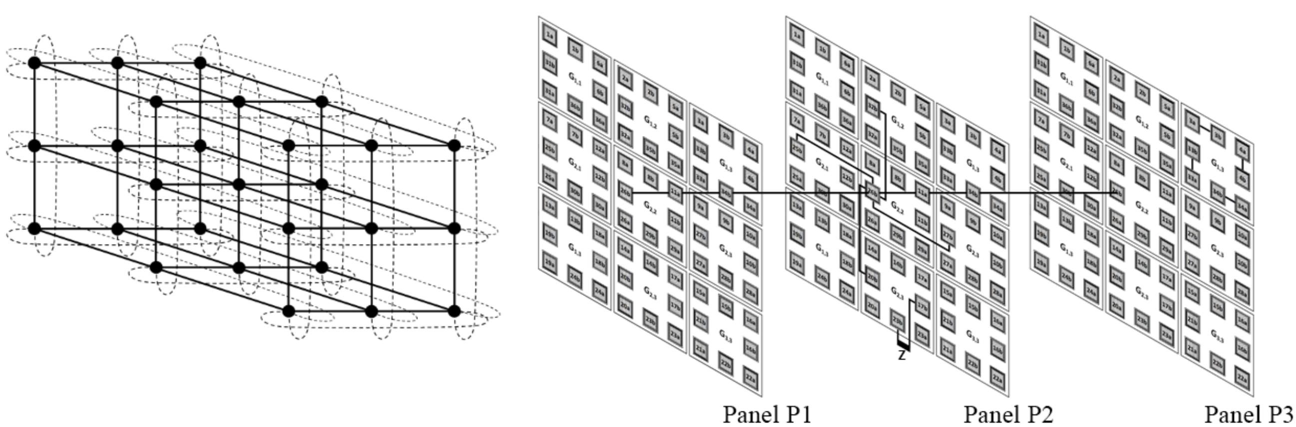

Fig. 5. Cell network with periodic boundary conditions (a) and system of connections between PCBs, which enables the system to be extended with periodic boundary conditions without a need to connect PCBs on the edge of the panels and on the outermost panels (b)

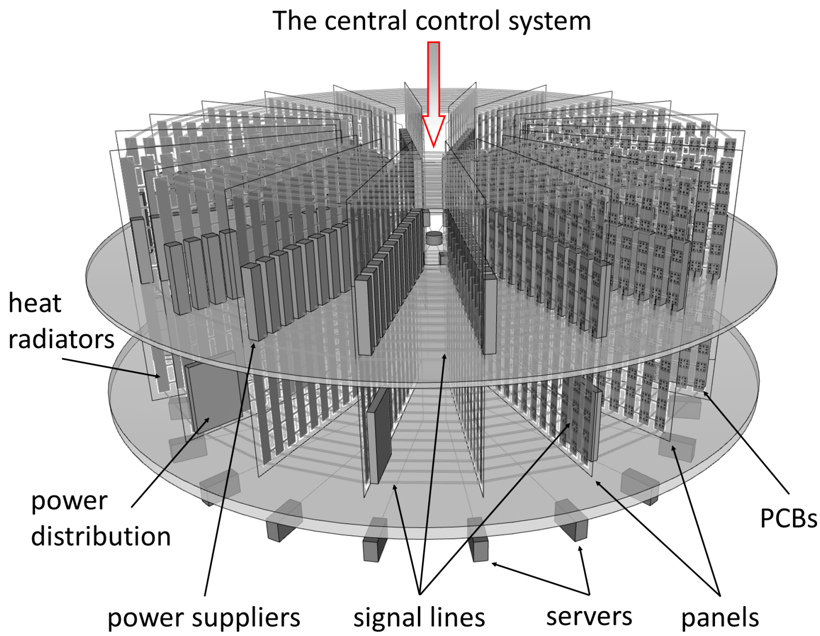

Fig. 6. Exemplary TAUR system design

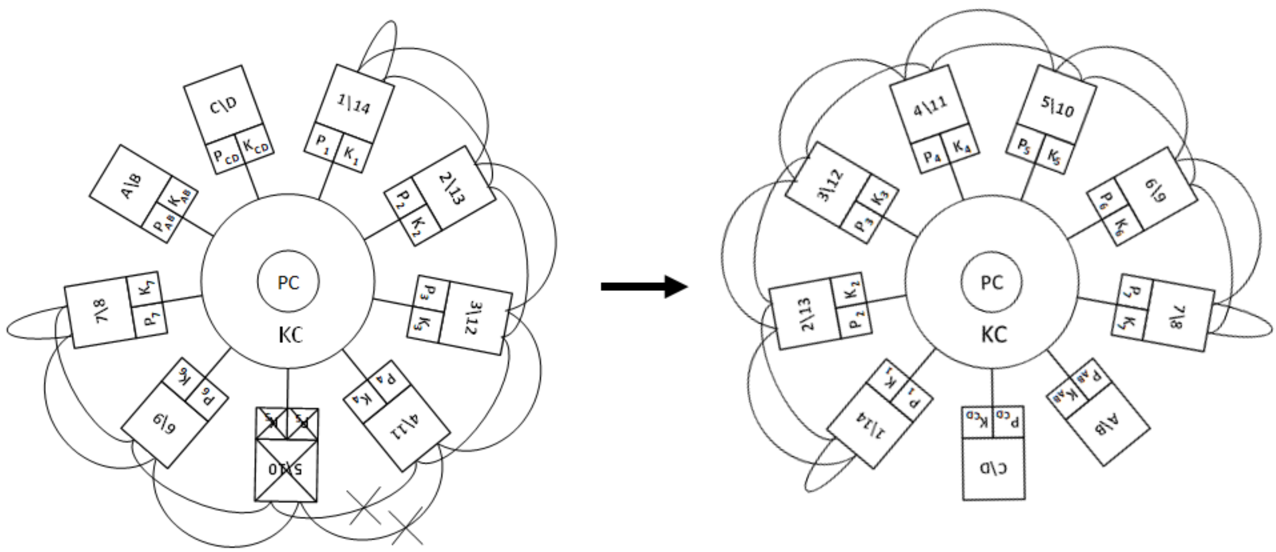

Fig. 7. Arrangement of panels in which 7 basic panels $(1/14, 2/13, \ldots, 7/8)$ and two additional panels (A/B) and (C/D) were used. This enables reconfiguration of the system in the event of a failure in one panel and/or signal lines connecting the pair of the other panels (a). Panels connections after the reconfiguration of the system as a result of failure of signal lines between the panels $(4/11)$ and $(5/10)$ (b)

III. PRACTICAL APPLICATION OF TAUR

In 2015, a system called the Analyzer of Real Complex Systems (ARUZ) [8] was constructed using TAUR in BioNanoPark Łódź laboratory complex (in the Laboratory of Molecular Simulations), which is presented in Fig. 8.

The specific architecture of ARUZ includes a dedicated operating system. The external data is delivered to FPGA devices via 240 channels connecting 12 PCBs (Fig. 9b), each arranged on 20 vertical panels (Fig. 9c) in 12 lines. In each of the FPGAs mounted on PCBs (Fig. 9a up to 256 operational cells are implemented. Signals are exchanged between neighboring cells via very fast 1Gb/s links. Results of data processing are collected through panel servers and are accessible for the system operators.

ARUZ contains the world's largest number of interconnected FPGAs, operation of which is controlled by 2.880 Linux operating systems simultaneously. The technical pa-

Fig. 8. The view of ARUZ located in the Laboratory of Molecular Simulations in BioNanoPark Łódź

rameters of ARUZ are: 25.920 Artix XC7A200T FPGAs and 2.880 Zynq XC7Z015 circuits; management infrastructure – 22 servers with NAS matrix; 500 kVA UPS; weight – 52 tons; dimensions – height 4.5 m, diameter 14 m; Faraday cage chasing – height 5.3 m, diameter 16 m (24-wall base), attenuation of 100 dB, filtered passages for fiber optic communication, power supply, ventilation, cooling system and gas extinguishing system; energy consumption – power consumption is about 100 kW for specific implemented computing algorithm, with infrastructure about 70 kW, theoretical maximum allowable power consumption is 500 kVA.

The ARUZ signal processing speed is very high. Measurements showed that the exemplary molecular simulation using the Dynamic Lattice Liquid (DLL) algorithm [9–10] for a molecular object containing 1.5 million molecules performing 10^{10} algorithm steps using a PC (i7-4930K@4.1GHz) will be performed within 40 years, estimates for the Prometheus supercomputer (Poland) are about 100 days, while ARUZ will perform the same task within 12 days [8, 10].

The TAUR technology is an original work performed at Lodz University of Technology as a result of many years of cooperation between the Department of Molecular Physics and the Department of Microelectronics and Computer Science. Currently, two research national projects are realized with the use of ARUZ (NCN grant 2014/14/A/ST5/00204 and NCN grant 2017/25/B/ST5/01970) concerning simulations of complex molecular systems containing from 1.5 million to 5 million molecules. First simulations on the ARUZ machine concerned polymer brushes, i.e. dense systems of chains grafted to a surfaces [9] and double polymer brushes [10] revealing information about the structure unattainable by other calculation tools.

Acknowledgment

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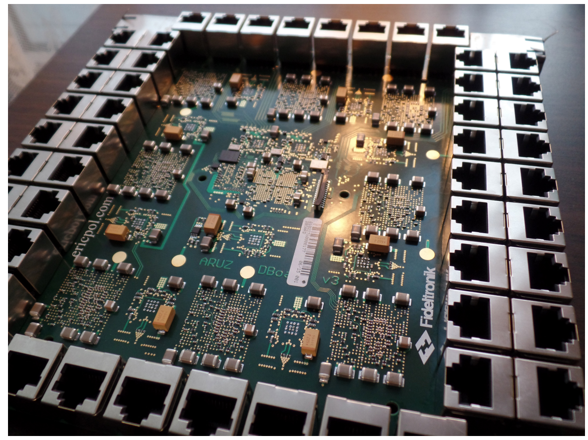
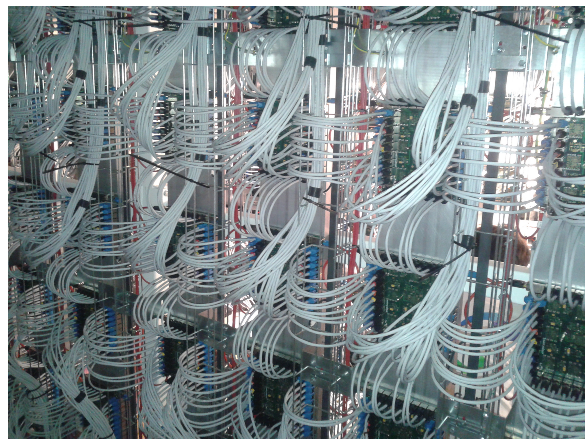


(a)



(b)

(c)

Fig. 9. Printed circuit boards with 8 FPGAs (a), communication lines to exchange data between neighboring FPGAs on PCBs (b) and vertically arranged flat panels containing PCBs (c)

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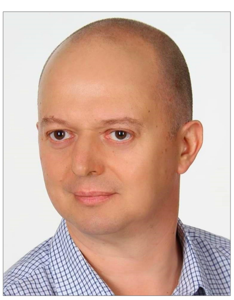
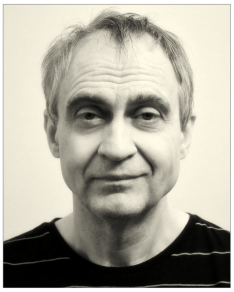


Rafał Kiełbik is an assistant professor at the Department of Microelectronics and Computer Science, Lodz University of Technology, Poland. In 2005 he received PhD degree for a dissertation on efficient methods of resource management in reconfigurable systems. His research focuses on inventing, developing and using reconfigurable devices for embedded systems as well as for general purpose and high performance computing.

Krzysztof Hałagan received his MSc in Physics in 2006 and his PhD degree in Chemical Technology in 2013, both from Lodz University of Technology. His main fields of interest are computer simulations of molecular systems using Monte Carlo methods, molecular dynamics and quantum calculations. His main research area includes application of the Dynamic Lattice Liquid algorithm to various physicochemical problems like diffusion, polymerization kinetics and simulation of soft matter, polymer systems and complex liquids. He is interested in hardware-related issues, accompanying computer modelling, like dedicated computing devices based on FPGAs and GPUs.



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Andrzej Sikorski graduated from the Department of Chemistry, University of Warsaw. He completed his PhD thesis in Chemistry in 1986 in the same Department. In 1987/89 and 1990/91, he worked as a postdoc and visiting professor at Washington University in St. Louis and in The Scripps Research Institute in La Jolla. In 1995, he obtained his DSc degree in Chemistry. His main scientific interests are: theory and simulations of polymers at interfaces and in confined geometries and molecular transport in a crowded environment.

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